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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,856	03/04/2004	Shigeru Shirayone	648.43608X00	5252

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EXAMINER	
KO, STEPHEN K	

ART UNIT	PAPER NUMBER
1792	

NOTIFICATION DATE	DELIVERY MODE
09/04/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/791,856	SHIRAYONE ET AL.	
	Examiner	Art Unit	
	STEPHEN KO	1792	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 May 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,8,9,14,16 and 17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,8,9,14,16 and 17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1, 3, 8-9 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitsunai et al (US 6,186,153) in view of Benzing (US 4,786,352) in further view of Collins et al (US 2003/0183243).

For claim 1, Kitsunai et al teach a method for removing deposition films which adhere to an inner wall of a semiconductor manufacturing apparatus (abstract) having a plasma generating means for generating plasma within a processing chamber, a high-frequency power supply (Fig.1, #11, col.3, L.52) for applying high-frequency power to an object to be processed, a processing chamber (Fig.1, #3 and #4 as a whole, col.3, L.40-41) to which an exhaust port (Fig.1, #10, col.3, L.42) is connected and which has its interior evacuated, and a gas introduction section (Fig.1, #15, col.3, L.43) for the processing chamber, said method comprising the steps of providing a period for cleaning an aluminum fluoride deposit in the semiconductor manufacturing apparatus by generating plasma containing BCl3 and Cl2 (read as removing an aluminum fluoride deposit adhered to the interior of the processing chamber by reaction between the aluminum fluoride deposit and plasma, col.5, L.37-42)

Kitsunai et al do not teach using hydrobromic gas.

Benzing teaches the equivalency of using a gas mixture of BCl3 and Cl2 with a gas mixture of HBr, Cl2, argon and an additional element (col.5, L.33-36).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the gas mixture of BCl3 and Cl2 of Kitsunai et al with a gas mixture of HBr, Cl2, argon and an additional element as mentioned Benzing

because the substitution of art recognized equivalents as shown by Benzing is within the level of ordinary skill in the art.

Kitsunai et al and Benzing do not teach the steps of mounting a Si wafer on an electrode for holding the object to be process; and generating a plasma while supplying Si atom to the plasma, the Si atoms being supplied to the plasma by applying the high-frequency power to the Si wafer, while the Si wafer is mounted on the electrode.

Collins et al teach a method for removing aluminum fluoride residues (paragraph [0042]) by providing a sacrificial substrate, including sacrificial material such as Silicon, on a support (read as mounting a Si wafer on an electrode for holding the object to be processed, paragraph [0043]); and providing and energizing sputtering gas such as argon by a plasma generator by applying a high-frequency power to the sacrificial wafer while the sacrificial substrate is mounted on the support in order to dislodge the sacrificial material species off the sacrificial substrate by bombarding the argon plasma to the sacrificial substrate(paragraph [0043]-[0046]). Since Kitsunai et al and Benzing teach removing deposition films which adhere to an inner wall of a semiconductor manufacturing apparatus by providing a plasma including argon gas and Collins et al teach a method for removing deposition films by supplying Si atom to a plasma with using the plasma including argon gas, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Kitsunai et al and Benzing by adding the steps of mounting a Si wafer on an electrode for holding the object to be process; and generating a plasma while supplying Si atom to the plasma, the Si atoms being supplied to the plasma by applying the high-frequency power to the

Si wafer, while the Si wafer is mounted on the electrode as motivated by Collins et al to facilitate cleaning (Collins et al, paragraph [0046]) with reasonable expectation of success.

For claims 3, and 8, Kitsunai et al teach a method for removing deposition films which adhere to an inner walls of a semiconductor manufacturing apparatus (abstract) comprising the steps of providing a period for cleaning an aluminum fluoride deposit in the semiconductor manufacturing apparatus by generating plasma containing BCl3 and Cl2 (read as create a gas phase reaction, col.5, L.37-42)

Kitsunai et al remain silent about the step of performing a cleaning step either each time after plasma processing a wafer or plural wafers or before and after plasma processing.

However, it is within the skills of the ordinary skilled in the art to establish the appropriate chamber cleaning schedule. Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Kitsunai et al by having a chamber cleaning step each time after plasma processing a wafer or plural wafers to prevent contamination of semiconductor wafer by residues remaining in the chamber upon processing.

Kitsunai et al do not teach using hydrobromic gas.

Benzing teaches the equivalency of using a gas mixture of BCl3 and Cl2 with a gas mixture of HBr, Cl2, argon and an additional element (col.5, L.33-36).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the gas mixture of BCl3 and Cl2 of Kitsunai et al with a

gas mixture of HBr, Cl2, argon and an additional element as mentioned Benzing because the substitution of art recognized equivalents as shown by Benzing is within the level of ordinary skill in the art.

Kitsunai et al and Benzing remain silent about the steps of supplying Si atoms to the plasma by placing a Si wafer, with no patterns printed thereon, on the substrate holder when the plasma is discharged; applying high frequency power to the Si wafer through the substrate holder, wherein the high frequency power being applied corresponds to a frequency of 400 kHz and is equal to or greater than 0.11W per unit area (1 cm2) of the Si wafer.

Collins et al teach a method for removing aluminum fluoride residues (paragraph [0042]) by providing a sacrificial substrate, including sacrificial material such as Silicon, on a support (read as mounting a Si wafer on an electrode for holding the object to be processed, paragraph [0043]); and providing and energizing sputtering gas such as argon by a plasma generator by applying a high-frequency power to the sacrificial wafer while the sacrificial substrate is mounted on the support in order to dislodge the sacrificial material species off the sacrificial substrate by bombarding the argon plasma to the sacrificial substrate(paragraph [0043]-[0046]).

Since Kitsunai et al and Benzing teach about removing deposition films which adhere to an inner wall of a semiconductor manufacturing apparatus by providing a plasma including argon gas and Collins et al teach a method for removing deposition films by supplying Si atom to a plasma with using the plasma including argon gas, it would have been obvious to one of ordinary skill in the art at the time the invention was

made to modify the method of Kitsunai et al and Benzing by adding the steps of mounting a Si wafer on an electrode for holding the object to be process; and generating a plasma while supplying Si atom to the plasma, the Si atoms being supplied to the plasma by applying the high-frequency power to the Si wafer, while the Si wafer is mounted on the electrode as motivated by Collins et al to facilitate cleaning (Collins et al, paragraph [0046]) with reasonable expectation of success

For claim 9, Regarding the high frequency power being applied corresponds to a frequency of 400 kHz and is equal to or greater than 0.11W per unit area (1 cm2) of the Si wafer, it is noted that these parameters are result effective, because they affect the efficiency and effectiveness for removing deposits and affect the cleaning result, and one skilled in the art would modify different variables to achieve optimum result, consult, *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

For claim 14, note that Kitsunai et al teach sequential execution of a cleaning operation using SF6 (read as providing a period for generating plasma containing SF6 prior to said period for generating plasma with the chlorine gas and hydrobromic gas, Kitsunai et al, col.5, L.46-47).

5. Claims 3 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Qian et al (US 6,136,211).

Qian et al teach a method for etching a substrate in an etching chamber, and simultaneously cleaning a surface of the etching chamber wall, wherein a portion of material constituting the chamber includes Si (col.7, L.15-16 and col.7, L.39) comprising the steps of placing a substrate on a chuck disposed within the etching chamber (Fig.2,

#145, col.7, L.57); providing a period for cleaning a residue deposited in the etching chamber by generating a plasma from gases including Cl2, HBR, N2, SiCl4 ??(col.8, L.55-58 and col.9, L.6-17) to remove various residue including fluorine (read as create a gas-phase reaction, col.1, L.32) each time after plasma processing a wafer (Fig.3). Note that the Si of the chamber or SiCl4 will provide a Si atom to the plasma as Qian et al teach a method having the steps as claimed.

Qian et al do not explicitly teach removing aluminum fluoride deposit. However, since the steps for removing residue from the etching chamber wall in Qian are similar to those instantly claimed, removing the aluminum fluoride deposits, would also be reasonably expected within the teaching of Qian.

Response to Arguments

6. Applicant's arguments with respect to claims 1, 3, 8-9, 14, and 16-17 have been considered but are moot in view of the new ground(s) of rejection.

7. In response to applicants' argument that Qian et al do not disclose nor would have suggested adding Si atoms to the plasma. Examiner's position is that since Qian et al teach a method for cleaning etch residues on a chamber surfaces having the steps as stated in claim 3 and additionally teach the steps of providing a portion of material constituting the chamber includes Si and/or the gases including SiCl4 (col.7, L.15-16; col.7, L.39 and col.8, L.55-58), Qian et al teach providing a Si atoms to the plasma.

8. In response to applicants' argument that the cleaning gas in Qian et al is different from the mixture of gases from which the plasma is generated. Examiner position is that since claim 3 requires "generating plasma **containing** chlorine gas and hydrobromic

gas and additionally Si atoms"; and Qian et al teach a cleaning process involving generating plasma containing chlorine gas and hydrobromic gas and additionally Si atoms, Qian et al clearly meet the recited limitation as claimed.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEPHEN KO whose telephone number is (571)270-3726. The examiner can normally be reached on Monday to Thursday, 7:30am to 5:30pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Kornakov can be reached on 571-272-1303. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SK
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